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EXAMINER	
CHENG, PETER L	
ART UNIT	**PAPER NUMBER**
2625	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/669,247	LEA ET AL.	
	Examiner	Art Unit	
	PETER L. CHENG	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Although not mentioned in applicants' remarks received on 4/24/2008, Examiner notes that claim 11 has also been amended. Per a telephonic inquiry with Peter Kraguljac (Reg. #38,520), it was confirmed on 6/23/2008 that applicant did amend claim 11.

Claim Objections

2. Claim 2 is objected to because of the following informalities:

- **Line 4: "the page frame memory"** lacks antecedent basis; assume applicant is referring to **the page frame buffer** cited in **claim 1, lines 5, 7 – 8**, and **12 – 13**;

  however, since the specification uses the term **page frame memory**, suggest replacing **page frame buffer** with **page frame memory** in **claims 1** and **7**;

3. Claim 3 is objected to because of the following informalities:

- **Lines 2 - 3: "the page frame memory"** lacks antecedent basis; assume applicant is referring to **the page frame buffer** cited in **claim 1, lines 5, 7 – 8**, and **12 – 13**;

however, since the specification uses the term **page frame memory**, suggest replacing **page frame buffer** with **page frame memory** in **claims 1** and **7**;

4. Claim 4 is objected to because of the following informalities:

- **Line 5: "the page frame memory"** lacks antecedent basis; assume applicant is referring to **the page frame buffer** cited in **claim 1, lines 5, 7 – 8**, and **12 – 13**;

however, since the specification uses the term **page frame memory**, suggest replacing **page frame buffer** with **page frame memory** in **claims 1** and **7**;

5. Claim 15 is objected to because of the following informalities:

- **Line 2:** it is assumed that applicant intended to cite **the first image data page** instead of **the image data page**;

6. Claim 20 is objected to because of the following informalities:

- **Line 3:** replace **a image data page** with **an image data page**;

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1 – 4, 6 - 8, 10 - 12, 16 – 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **SHISHIZUKA [US Patent 6,697,898 B1]** in view of **WESTERVELT [US Patent Application 2003/0231330 A1].**

As for claim 1, SHISHIZUKA teaches an image forming device comprising:

a scanner configured to scan one or more objects and generate image data representing each of the one or more objects

[Fig. 2, scanner **203**; **Fig. 4** also shows an interface to the scanner labeled "VIDEO I/F TO SCANNER" from the "DoEngine"**];**

a memory configured to store each of the image data as a page of data

[Fig. 108, RAM **203a** which contains "PAGE MEMORY" **511** shown in **Fig. 111;** also referred to as "SDRAM"; **col. 66, line 50];**

a page frame buffer configured to store *~~a page of~~* data, copied from the memory, that is to be imaged

[SHISHIZUKA teaches a "page frame buffer" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine"**];**

an imaging mechanism configured to receive the page of data from the page frame buffer and generate an image from the page of data onto a print media

[Fig. 111, Printer **512; Fig. 4** also shows an interface to the printer labeled "VIDEO I/F TO PRINTER" from the "DoEngine"**];**

and a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism

[The DoEngine is a "single-chip scanning and printing engine"; **col. 6, lines 57 – 58.** It has "two independent buses in its chip, namely an IO bus (B bus) which connects universal IO core and a graphics bus (G bus) which is optimized to transfer … image data"; **col. 7, lines 21 – 24.**

With reference to **Fig. 91,** SHISHIZUKA illustrates a "copy mode in which an image is copied by transferring image data from the scanner controller to the printer controller by way of a memory"; **col. 5, lines 51 – 54.**

SHISHIZUKA teaches, "The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 44 – 46.** The GBI_SCC (i.e., the scanner G bus/B bus interface) "performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 *into the SDRAM*"; **col. 66, lines 46 – 50.**

"When an amount of the image data written into the SDRAM reaches to a level sufficient to buffer a difference between the data transfer speeds of the scanner

and the printer, image data transfer to the printer is started"; **col. 66, lines 50 – 53.**

"The printer controller (PRC) transfers the image data to the printer. By the DMA transfer of the GBI_PRC" (i.e., the printer G bus/B bus interface), "the *printer controller (PRC)* inputs the image data written in the SDRAM sequentially into the *internal FIFO*. Simultaneously, the printer controller (PRC) outputs the vertical synchronous signal (VSYNC) to the printer. Thereafter, the horizontal synchronous signal (HSYNC) and the video clock are input from the printer. In synchronization with the HSYNC and the video clock, the printer controller *outputs the image data from the internal FIFO to the printer*"; **col. 66, lines 58 – 67.**

Therefore, SHISHIZUKA teaches a first bus (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) which *is* connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) which connects the "scanner to the memory" and a second bus (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**) which connects the "page frame buffer to the imaging

mechanism". Data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.**]**

However, SHISHIZUKA does not specifically teach

a page frame buffer configured to store a *page* of data

WESTERVELT teaches a "page frame buffer" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and configure a "page frame buffer" to store an amount of data in the page frame buffer to maintain a balance between a level of system performance for the intended imaging mechanism and system cost.

Regarding claim 2, SHISHIZUKA further teaches the device of claim 1 where

the dual bus system includes a first bus ~~configured~~ connected to communicate data between the scanner and the memory

[As noted for claim 1, this bus extends from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) *and is* connected to SDRAM by means of a "System Bus Bridge" **402**, "MC Bus", "SDRAM & ROM Controller (MC)" **403**, and "Memory BUS", all shown in **Fig. 4]**,

and a second bus, independent from the first bus, connected ~~configured~~ to communicate data between the page frame memory and the imaging mechanism

[As noted for claim 1, this bus extends from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4].**

Regarding claim 3, SHISHIZUKA further teaches the device of claim 2 where

the first bus is configured to allow image data to be loaded into the memory independent of transmitting data from the page frame memory to the imaging mechanism

[As noted for claim 1, once the page frame buffer contains data for the imaging mechanism, data can be sent from the page frame buffer (i.e., the printer controller's FIFO) independently of and simultaneously with loading image data

from the scanner to the "memory" since the first bus and second bus are separate**].**

Regarding claim 4, SHISHIZUKA further teaches the device of claim 2 further comprising:

a first processor configured to control communication of the image data to the memory

[Fig. 4, scanner controller **4302]**;

and a second processor configured to control communication of the page of data from the page frame memory to the imaging mechanism

[Fig. 4, printer controller **4303].**

Regarding claim 6, SHISHIZUKA further teaches the device of claim 4 where

the first and second processors include application specific integrated circuits

[Both first (i.e., scanner controller) and second (i.e., printer controller) processors are contained in the "DoEngine" application-specific IC (ASIC). "The DoEngine is a large-scale ASIC"; **col. 63, line 35].**

Regarding claim 7, SHISHIZUKA *does not specifically teach* the device of claim 1 where

the page frame buffer is configured to store *one or more pages of data* as one or more units

However, as noted for claim 1, WESTERVELT teaches that a printer controller FIFO may store a "scanline, band, page or plane" of data at a time.

Regarding claim 8, SHISHIZUKA further teaches the device of claim 1 where

the dual bus system is configured to communicate data by direct memory access

["The GBI_SCC performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 into the SDRAM"; **col. 66, lines 46 – 50.**

"By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO"; **col. 66, lines 59 - 61].**

Regarding claim 10, SHISHIZUKA further teaches the device of claim 1 where

the page of data includes at least three planes of color data

[Fig. 44, video RGB (red, green, blue) image data from the "scanner device I/F" **4401].**

Regarding claim 11, SHISHIZUKA teaches a method of processing image data in an image forming device, the method comprising:

scanning one or more sheets of print media and generating one or more image data pages;

loading the one or more image data pages into a memory;

[SHISHIZUKA teaches, "The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 44 – 46.** The GBI_SCC (i.e., the scanner G bus/B bus interface) "performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 *into the SDRAM*"; **col. 66, lines 46 – 50.]**

copying a first image data ~~page~~ into a page frame memory from the memory to prepare for imaging

["When an amount of the image data written into the SDRAM reaches to a level sufficient to buffer a difference between the data transfer speeds of the scanner and the printer, image data transfer to the printer is started"; **col. 66, lines 50 – 53.**

"The printer controller (PRC) transfers the image data to the printer. By the DMA transfer of the GBI_PRC" (i.e., the printer G bus/B bus interface), "the *printer*

controller (PRC) inputs the image data written in the SDRAM sequentially into the *internal FIFO*"; **col. 66, lines 58 – 61];**

and transmitting the first image data page for imaging to an imaging mechanism where the transmitting ~~can~~ occurs in parallel with the loading **[**"Simultaneously, the printer controller (PRC) outputs the vertical synchronous signal (VSYNC) to the printer. Thereafter, the horizontal synchronous signal (HSYNC) and the video clock are input from the printer. In synchronization with the HSYNC and the video clock, the printer controller *outputs the image data from the internal FIFO to the printer*"; **col. 66, lines 62 – 67.**

Therefore, SHISHIZUKA teaches a first bus (i.e., either of the G bus or B bus which is connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) which connects the "scanner to the memory" and a second bus (i.e., from the FIFO contained within the "Printer Controller" **4303** to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**) which connects the "page frame buffer to the imaging mechanism". Data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.**]**

However, SHISHIZUKA does not specifically teach

copying a first image data *page* into a page frame memory from the memory to prepare for imaging

WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and configure a "page frame buffer" to store an amount of data in the page frame buffer to maintain a balance between a level of system performance for the intended imaging mechanism and system cost.

Regarding claim 12, SHISHIZUKA further teaches the method of claim 11 further including

converting the first image data page into print ready data before transmitting for imaging

[As shown in **Fig. 68**, Printer Video Clock Unit **6602** converts 64-bit image data to 24-bit RGB image data; a "Printer Video Data Width Converter" **6083** "is a

block which converts image data sent in a 64-bit width from the I/F bus into RGB 24 bits, white-black 8 bits and white-black 1 bit dependently on a mode"; **col. 42, lines 42 - 46].**

Regarding claim 16, SHISHIZUKA further teaches the method of claim 11 further including

sequentially copying ~~the one or more image~~ data ~~pages~~ from the memory to the page frame memory to prepare for imaging

[SHISHIZUKA teaches a "page frame buffer" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller **6603**. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18**. As shown in **Fig. 66**, the FIFO controller **6603** is a component of the "printer controller" **4303**; **col. 4, line 61**. As shown in **Fig. 4** and **Fig. 91**, the "printer controller" **4303** is a component of the "DoEngine"**].**

However, SHISHIZUKA does not specifically teach

sequentially copying the *one or more image data pages*

As noted for claim 11, WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and configure a "page frame buffer" to store an amount of data in the page frame buffer to maintain a balance between a level of system performance for the intended imaging mechanism and system cost.

Regarding claim 17, SHISHIZUKA teaches a system for formatting image data for an image forming device, the system comprising:

a first data bus

[As noted for claim 1, this bus extends from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) *and is* connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4];**

a first memory configured to store image data pages, the first memory being configured to receive the image data pages over the first data bus [Fig. 108, RAM **203a** which contains "PAGE MEMORY" **511** shown in **Fig. 111;** also referred to as "SDRAM"; **col. 66, line 50];**

a second memory configured to load ~~a page of~~ data that is to be imaged, the ~~page of~~ data being received from the first memory
[SHISHIZUKA teaches a "page frame buffer" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine"**];**

and a second data bus configured to communicate the page of data from the second memory to an imaging mechanism
where the page of data can be transmitted to the imaging mechanism in parallel with the first memory receiving the image data pages.

[As noted for claim 1, this bus extends from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4.**

Since the first and second data busses are separate, data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.**]**

However, SHISHIZUKA does not specifically teach

a second memory configured to load *a page of data* that is to be imaged, the *page of data* being received from the first memory

WESTERVELT teaches a "page frame buffer" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and configure a "page frame buffer" to store an amount of data in the page frame buffer to

maintain a balance between a level of system performance for the intended imaging mechanism and system cost.

Regarding claim 18, SHISHIZUKA further teaches the system as set forth in claim 17 further including

> **an imaging processor configured to process the page of data from the second memory into print ready data that can be processed by the imaging mechanism**
>
> **[**As shown in **Fig. 68**, Printer Video Clock Unit **6602** converts 64-bit image data to 24-bit RGB image data; a "Printer Video Data Width Converter" **6083** "is a block which converts image data sent in a 64-bit width from the I/F bus into RGB 24 bits, white-black 8 bits and white-black 1 bit dependently on a mode"; **col. 42, lines 42 - 46].**

Regarding claim 19, SHISHIZUKA further teaches the system as set forth in claim 18 where

> **the imaging processor includes one or more logic circuits each configured to process one plane of color data from the page of data**
>
> **[**As shown in **Fig. 68**, Printer Video Clock Unit **6602** converts 64-bit image data to 24-bit RGB image data; a "Printer Video Data Width Converter" **6083** "is a block which converts image data sent in a 64-bit width from the I/F bus into RGB

24 bits, white-black 8 bits and white-black 1 bit dependently on a mode"; **col. 42, lines 42 – 46.**

Fig. 71A and **Fig. 71B** illustrate separate functional blocks which produce the above-mentioned "RGB" (red, green, blue) and "B/W" (black and white) printer data**].**

Regarding claim 20, SHISHIZUKA further teaches the system as set forth in claim 17 where

the first data bus is in data communication with a scanning device configured to scan objects and generate an image data page including color data representing each scanned object

[Fig. 2, scanner **203**; also, shown in **Fig. 4** is a "VIDEO I/F TO SCANNER"; the first bus extends from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) *and is* connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4.**

Fig. 44 show a block diagram of the scanner controller (**Fig. 4** Scanner Controller **4302**) and illustrates color RGB 8-bit data being acquired from the "Scanner Device I/F" **4401].**

Regarding claim 22, SHISHIZUKA further teaches the system as set forth in claim 17 where

the system is configured to copy an image data page from the first memory to the second memory by direct memory access

["The GBI_SCC performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 into the SDRAM"; **col. 66, lines 46 – 50**. "By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO"; **col. 66, lines 59 - 61].**

Regarding claim 23, SHISHIZUKA further teaches the system as set forth in claim 17 where

the system is configured to process image data pages as one or more data units

[Fig. 111 shows the "detailed software structure of the peripheral device in the information processing system" and how the software creates "jobs". With reference to **Fig. 111**, SHISHIZUKA further teaches a "composite copying job" which is "divided into a scanning job and printing job"; **col. 72, lines 38 – 39**. Further, "a device is assigned to the divided job in units of pages to process the job" (**col. 72, lines 40 – 42**)**].**

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 5, 9, 13, 14, 15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **SHISHIZUKA [US Patent 6,697,898 B1]** in view of **WESTERVELT [US Patent Application 2003/0231330 A1]** in view of well-known prior art**.**

Regarding claim 5, SHISHIZUKA *does not specifically teach* the device of claim 4 where

> **the second processor is configured to decompress the page of data and transmit pulse modulated wave patterns to the imaging mechanism based on the decompressed page of data**

However, SHISHIZUKA does teach that the "DoEngine can be combined with a rendering engine having a PCI bus interface and a compression/elongation engine"; **col. 7, lines 18 – 20**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a compression/de-compression engine in order to efficiently use available RAM and external storage (e.g. a hard disk).

Regarding claims 9, SHISHIZUKA *does not specifically teach* the device of claim 1 further including

> **a storage device *configured to store image data from the scanner once the memory is full*.**

In **Fig. 108**, SHISHIZUKA shows an "external storage device" **204a** "such as a hard disk" (**col. 70, lines 64 – 67**) and teaches that it may be used to store scanned image data; **col. 72, lines 9 – 10.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the storage disk device to "store overflow image data pages after the first memory is at capacity".

Regarding claim 13, SHISHIZUKA *does not specifically teach* the method of claim 11 further including

holding the first image data page in the page frame memory until the imaging mechanism is ready to print.

However, SHISHIZUKA does teach that the print controller control register 6604 includes a "printer device status register"; **col. 44, line 45.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to check the printer device status register and confirm that the printer was in a state to receive data. For example, if the printer were in an error state (e.g. a paper jam), image data would be held in the page frame memory until the error condition cleared.

Regarding claim 14, SHISHIZUKA *does not specifically teach* the method of claim 11 further including

loading one or more image data pages into a mass storage device once the memory is full.

In **Fig. 108**, SHISHIZUKA shows an "external storage device" **204a** "such as a hard disk" (**col. 70, lines 64 – 67**) and teaches that it may be used to store scanned image data; **col. 72, lines 9 – 10.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the storage disk device to "store overflow image data pages after the first memory is at capacity".

Regarding claim 15, SHISHIZUKA *does not specifically teach* the method of claim 11 further including

> **removing an image data page from the memory after the image data page has been imaged and outputted from the image forming device.**

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to either remove or overwrite the image data from memory in order to re-use the memory for subsequent pages.

Regarding claim 21, SHISHIZUKA *does not specifically teach* the system as set forth in claim 17 further including

> **a storage disk device *configured to store overflow image data pages after the first memory is at capacity***

In **Fig. 108**, SHISHIZUKA shows an "external storage device" **204a** "such as a hard disk" (**col. 70, lines 64 – 67**) and teaches that it may be used to store scanned image data; **col. 72, lines 9 – 10.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the storage disk device to "store overflow image data pages after the first memory is at capacity".

Response to Arguments

13. Applicant's arguments filed 4/24/2008 have been fully considered but they are not fully persuasive.

Regarding claim 1, with respect to applicant's argument that

> *the "arrangement of elements and configuration of the dual bus is not taught or suggested by references";* **page 11, 4th paragraph.**
>
> *"A page frame buffer (being a separate element from the cache memory 403) is not present and not part of the G bus and B bus configuration. Thus, the claimed page frame buffer and the claimed arrangement with the recited dual bus system is not taught by the G and B buses of SHISHIZUKA";* **page 11, 5th paragraph.**

has been considered.

In reply,

> As noted in the claim rejection, SHISHIZUKA cites, "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine".
>
> SHISHIZUKA's "printer FIFO" (i.e., "page frame buffer") is contained in a printer image data transfer FIFO controller 6603 which, in turn, is *connected to the G and B buses by means of the GBI (G bus/B bus I/F) interface*.

Regarding claim 1, with respect to applicant's argument that

> *"Thus the first and second buses explained by the Office Action comprise multiple components connected by interface ports (e.g. I/F) and multiple communication paths, none of which teaches the dual bus that can transmit image data from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism";* **page 12, 5th paragraph.**

and regarding the "scanner video I/F connections and components" shown in ***Fig. 45*** *of SHISHIZUKA and the "printer controller 4303 components and connections including the printer device I/F" shown in* ***Figs. 66 – 67****of SHISHIZUKA, the multiple channels and paths relied upon by the examiner cannot constitute a first or second bus, and fail to teach or suggest a first bus and a second bus as proposed by the Office Action";* **page 12, 5th paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches a first bus (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) which is connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) which connects the "scanner to the memory" and a second bus (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**) which connects the "page frame buffer to the imaging mechanism". Data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.

SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

With this configuration and with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

It should be noted that SHISHIZUKA provides detail at a lower "functional block level", whereas, applicant's **Figs. 1** and **2** are higher "system level diagrams". Therefore, care should be taken when comparing the two inventions.

For example, even though SHISHIZUKA's first and second buses comprise "multiple components", the applicant also has indicated that "*it will be appreciated that any number and configuration of data busses may be used to accommodate desired functions or preference. The operation and directional flow of the image data will be further explained with reference to Figure 2*"; **page 8, lines 6 – 8.**

This appears to be an admission that the actual implementation of the higher-level "system diagrams" may require additional components.

For example, applicant's "second bus" **185** shown in **Fig. 1** is illustrated as being composed of *one section* between the "page frame memory" **170** and an "imaging processor" **180** (which converts the data page from the page frame memory **170** to a "print ready engine format"; **page 7, lines 1 - 3**), and *another section* between the "imaging processor" **180** and "imaging mechanism" **130.**

Access to a memory is typically made by use of a "memory bus" consisting of address, data and control lines, whereas, *communications* with an "imaging mechanism" is typically made by a bus consisting of data and control lines. This suggests that the two sections of the "second bus" may not be the same.

Similarly, applicant's "first bus" **155** shown in **Fig. 1** is illustrated as being composed of *one section* between the "scanner" **110** and the "controller" **140**, and *another section* between the "controller" **140** and the "main memory" **150**. As noted, access to a memory is typically made by use of a "memory bus" consisting of address, data and control lines, however, applicant also suggests that "data pages can then be sent and loaded into a formatter 120 by, for example, a FIREWIRE® bus or other type of bus using another desired communication protocol"; **page 4, lines 25 – 27.**

Regarding claim 1, with respect to applicant's argument that

> *the statement cited in the previous action on* ***page 6, last paragraph****, "'data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer' is not supported by SHISHIZUKA and no citation to an actual teaching in SHISHIZUKA is provided. Accordingly, SHISHIZUKA fails to teach or suggest the elements relied upon by the rejection";* **page 13, 1st paragraph.**

has been considered.

In reply,

> As noted above, SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**
>
> Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different

from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 1, with respect to applicant's argument that

"WESTERVELT fails to teach or suggest how its FIFO buffer would be connected and where it would be connected into the DoEngine of SHISHIZUKA. Indeed the DoEngine already includes a cache memory 403 (figure 4) and the printer controller 4303 already includes a FIFO buffer 6608 (figure 66)"; **page 13, 2nd paragraph.**

"Thus, the motivation to combine provided by the Office Action (page 7, 3rd paragraph) is not supported by the references. Rather, the combination is made using impermissible hindsight using the claims as a blueprint. The rejection is improper"; **page 13, 2nd paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches a "page frame buffer" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a

buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine".

WESTERVELT teaches a "page frame buffer" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.**

Since SHISHIZUKA does not specifically teach a page frame buffer (i.e., the "printer FIFO") as being configured to store *a page of data*, the WESTERVELT reference teaches that the size of the "printer FIFO" can be made to accommodate not only pages of data but also scanlines, bands or planes of data. That is, it would have been obvious to one of ordinary skill in the art at the time the invention was made to match the size of the "printer FIFO" with the "imaging mechanism". For example, laser printers require page-sized memories, whereas, a scanning inkjet printer would require a smaller band-sized memory.

Regarding claim 1, with respect to applicant's argument that

*the previous office action's citation of SHISHIZUKA's timing signals VSYNC and HSYNC signals on **pages 5 - 6** fails to "teach or suggest simultaneous or parallel transmission of data by a dual bus transferring data from page memory to the*

imaging mechanism while also transferring image data from a scanner to main memory"; **page 14, 1st paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches that "the image data is output in synchronization with these signals. The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 43 – 46.**

As noted above, SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 2, with respect to applicant's argument that

> *"no such first or second bus is taught or suggested.";* **page 14, 2nd paragraph.**

has been considered with respect to **claim 1**.

Regarding claim 11, with respect to applicant's argument that

> *the previous office action's citation of SHISHIZUKA's timing signals VSYNC and HSYNC signals on* ***page 12*** *"are not image data pages that are generated from scanning sheets of print media as recited in the claim, and the timing signals are not image data pages loaded into a memory";* **page 15, 2nd paragraph.**
>
> *"As such, the VSYNC and HSYNC timing signals, as well as the processing of the timing signals, are irrelevant to the claimed elements. Thus, the cited text fails to teach or suggest 'transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading' as recited in claim 11";* **page 15, 3rd paragraph.**

has been considered.

In reply,

As noted for claim 1, SHISHIZUKA teaches that "the image data is output in synchronization with these signals. The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 43 – 46.**

As previously noted, SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 17, with respect to applicant's argument that

"SHISHIZUKA fails to teach or suggest the recited arrangement of a first data bus, a second data bus, and parallel transmission of data between components as recited in claim 17"; **page 16, 1st paragraph.**

With regards to WESTERVELT's teaching a FIFO buffer, "as explained under claim 1, the combined references still fail to establish a prima facie obviousness rejection"; **page 15, 2nd paragraph.**

has been considered with respect to **claims 1** and **2**.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- U.S. Patent 5,864,652
- U.S. Patent 6,222,636
- U.S. Patent 6,226,102

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 571-272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/King Y. Poon/
Supervisory Patent Examiner, Art Unit 2625

plc
June 23, 2008